MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC68HC811E2

Technical Summary
8-Bit Microcontroller

Introduction

The MC68HC811E2 high-performance microcontroller (MCU) is based on the MC68HC11E9, but has one-half the RAM (256 bytes) and four times the EEPROM (2K bytes). The MC68HC811E2 is a high-speed, low-power chip that has a multiplexed bus, capable of operating at up to 2 MHz, and a fully static design that allows it to operate at frequencies down to dc.

For detailed information about subsystems, programming, and the instruction set, refer to the *M68HC11 Reference Manual*, document number M68HC11 RM/AD.

Features

- MC68HC11 CPU
- Power Saving STOP and WAIT Modes
- 2K Bytes of On-Chip EEPROM With Block Protect for Extra Security
- 256 Bytes of On-Chip RAM, All Saved During Standby
- 16-Bit Timer System
  - — Four Output Compare Channels
  - — Three Input Capture Channels
  - — One Input Capture or Output Compare (Software Selectable)
- 8-Bit Pulse Accumulator
- Real-Time Interrupt Circuit
- Computer Operating Properly (COP) Watchdog System
- Synchronous Serial Peripheral Interface (SPI)
- Asynchronous Nonreturn to Zero (NRZ) Serial Communications Interface (SCI)
- 8-Channel 8-Bit Analog-to-Digital (A/D) Converter
- 38 General-Purpose I/O Pins
  - — 16 Bidirectional Input/Output (I/O) Pins
  - — 11 Input-Only Pins and 11 Output-Only Pins
- Available in a 52-Pin Plastic Leaded Chip Carrier (PLCC), or a 48-Pin Dual-In-Line Package (DIP)

Ordering Information

Package	Temperature	CONFIG	MC Order Number
52-Pin PLCC (FN suffix)	– 40° to + 85°C	$FF	MC68HC811E2FN
	– 40° to + 105°C	$FF	MC68HC811E2VFN
	– 40° to + 125°C	$FF	MC68HC811E2MFN
48-Pin DIP (P suffix)	– 40° to + 85°C	$FF	MC68HC811E2P
	– 40° to + 105°C	$FF	MC68HC811E2VP
	– 40° to + 125°C	$FF	MC68HC811E2MP

MOTOROLA

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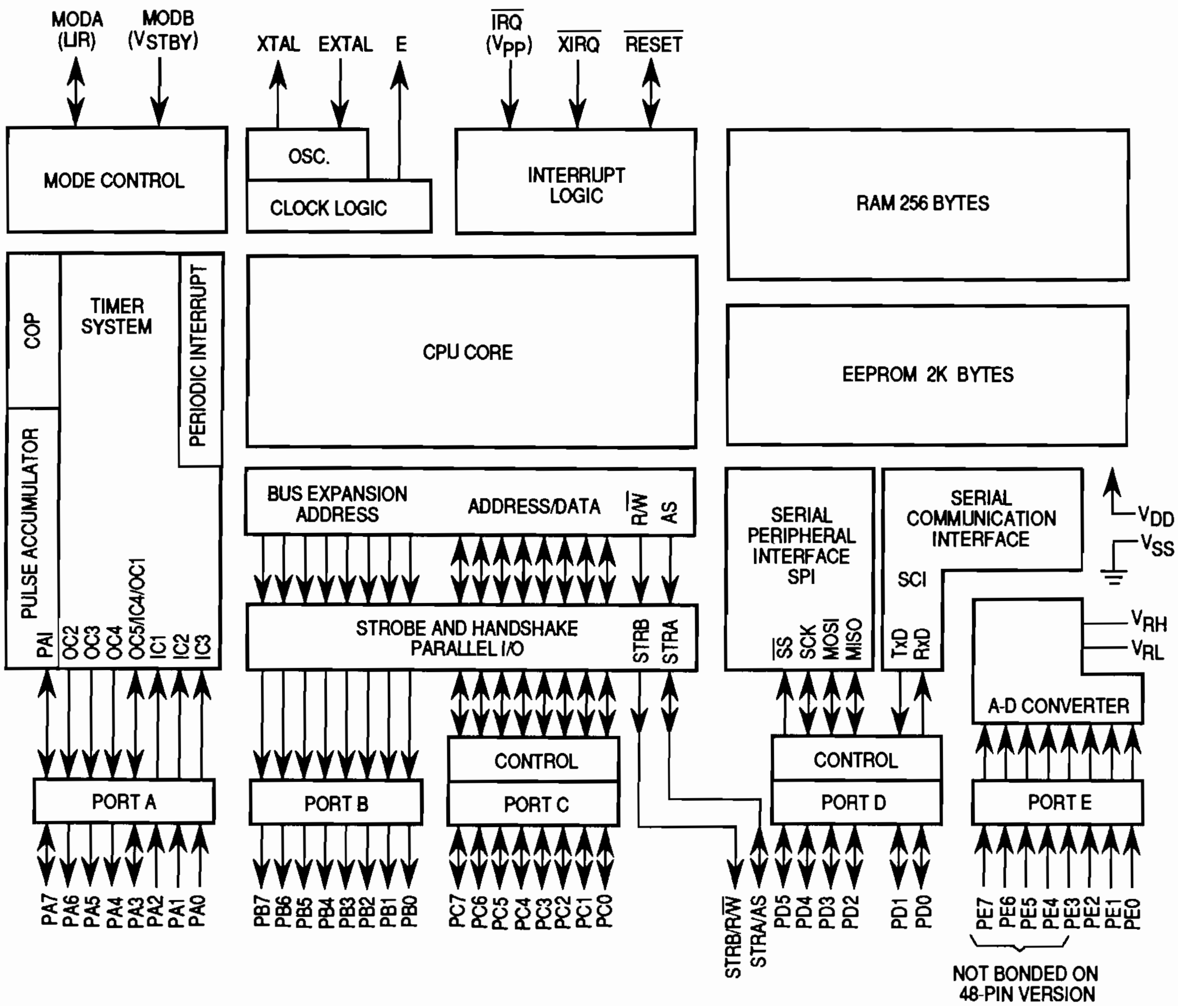
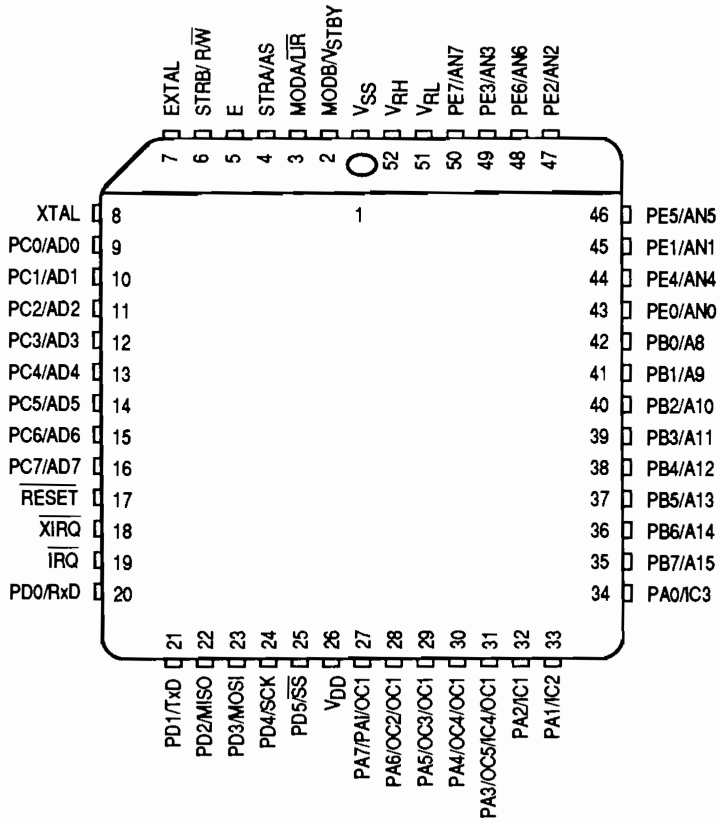
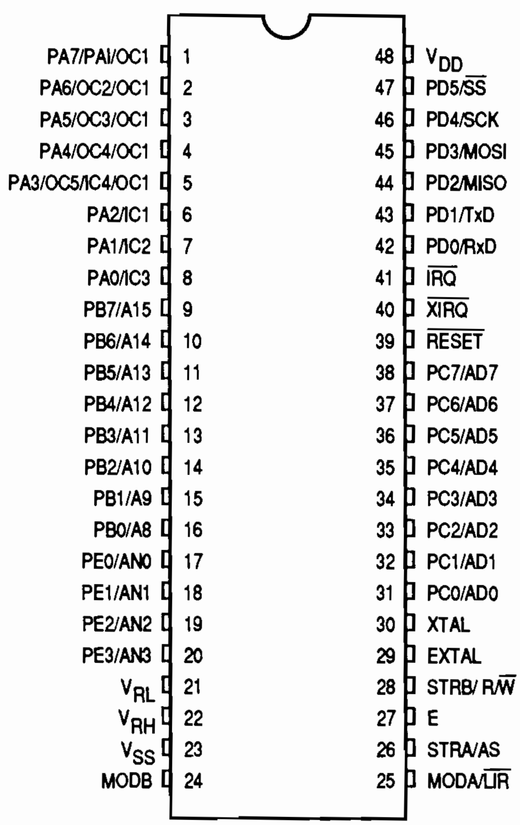


Block Diagram



PLCC Pin Assignments

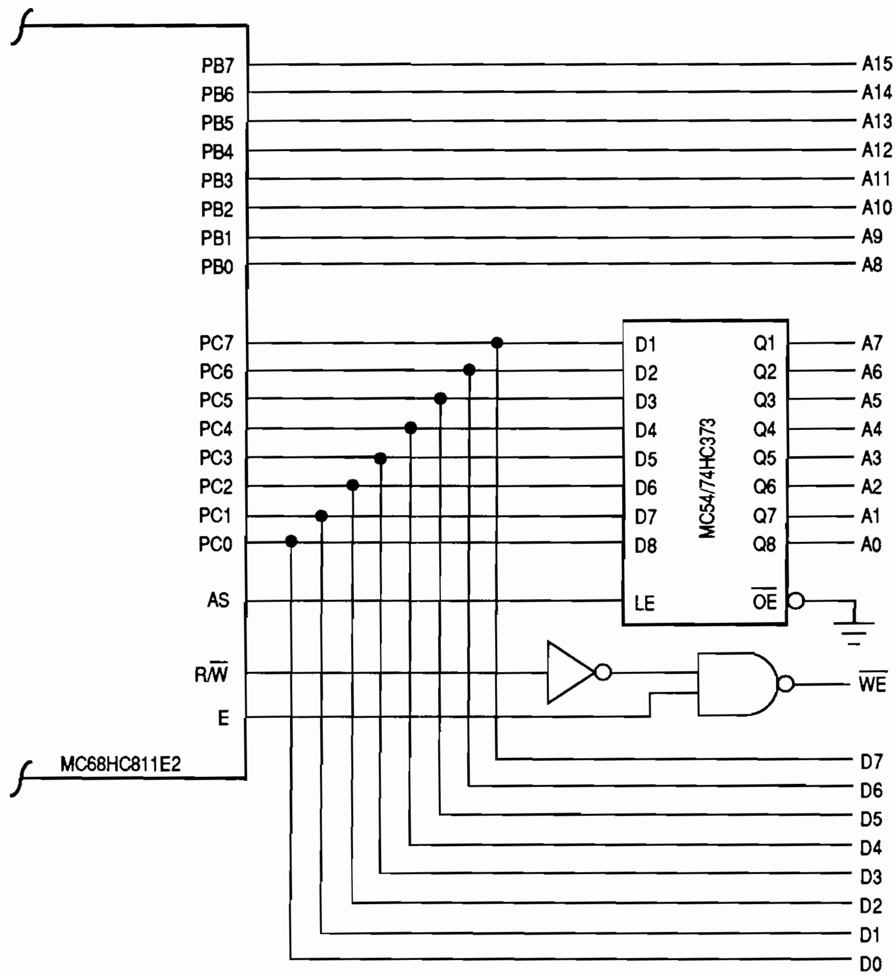


DIP Pin Assignments

Operating Modes and Memory Maps

In single-chip operating mode, the MC68HC811E2 is a monolithic microcontroller without external address or data buses.

In expanded multiplexed operating mode, the MCU can access a 64K-byte address space. The space includes the same on-chip memory addresses used for single chip mode, in addition to external peripheral and memory devices. The expansion bus is made up of ports B and C and control signals AS and R/$\overline{W}$. The address, R/$\overline{W}$, and AS signals are active and valid for all bus cycles including accesses to internal memory locations. The following figure illustrates a recommended method of demultiplexing low order addresses from data at port C.



Address/Data Demultiplexing

Special bootstrap mode allows quantities of special purpose programs to be entered into internal RAM. The boot loader program uses the SCI to read a 256-byte program into on-chip RAM at \$0000 through \$00FF. After receiving the character for address \$00FF, control passes to the loaded program at \$0000.

Special test mode isused primarily for factory testing.

Memory Maps

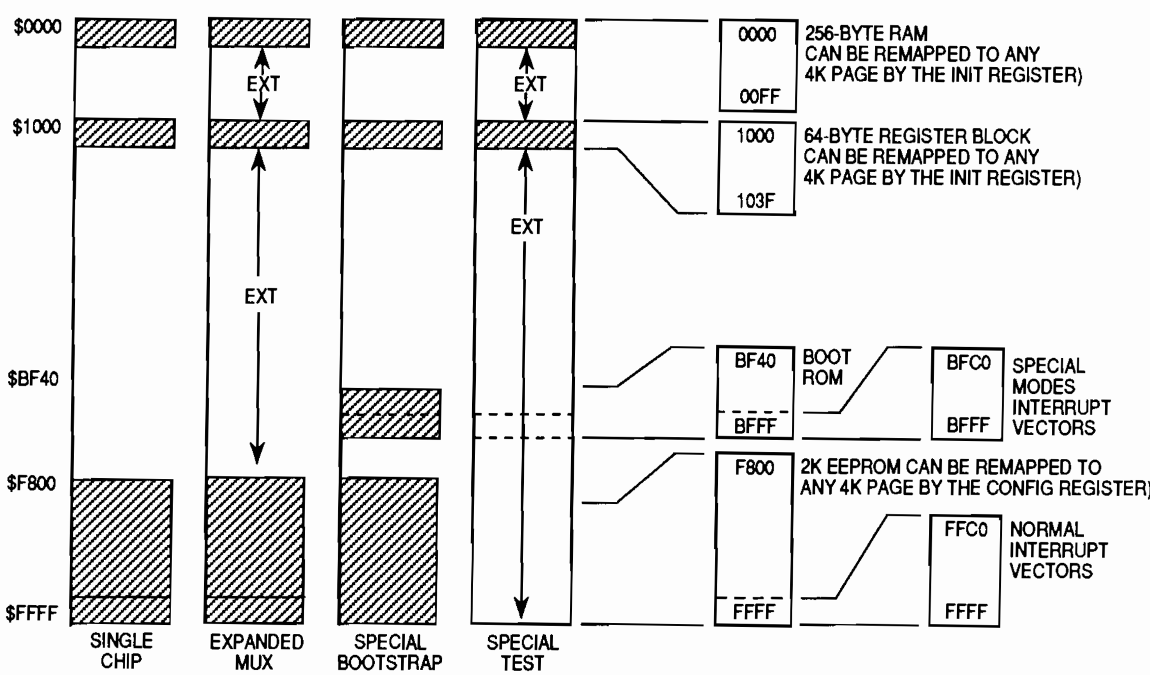
Memory locations are the same for both expanded multiplexed and single-chip modes. The 64-byte register block originates at $1000 after reset and can be placed at any other 4K boundary ($x000) after reset by writing an appropriate value to the INIT register. The 256-byte RAM originates at $0000 after reset and can be placed at any 4K boundary by writing the appropriate value to the INIT register.

The 2K-byte EEPROM is initially located at $F800 through $FFFF in single chip mode after reset, if it is enabled. In all other modes its position depends on the EE3–EE0 bits in the CONFIG register and whether or not the EEON bit is set.

Hardware priority is built into the memory remapping. Registers have priority over RAM and boot ROM has priority over EEPROM. The higher priority resource covers the lower, making the underlying locations inaccessible.

In special bootstrap mode, a bootloader ROM is enabled at locations $BF40 through $BFFF.

In special test mode and special bootstrap mode, reset and interrupt vectors are located at $BFC0 through $BFFF.



Memory Map

Registers (1 of 2)

(The register block can be remapped to any 4K boundary.)

	Bit 7	6	5	4	3	2	1	Bit 0	
$1000	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	PORTA
$1001									Reserved
$1002	STAF	STAI	CWOM	HNDS	OIN	PLS	EGA	INVB	PIOC
$1003	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	PORTC
$1004	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	PORTB
$1005	PCL7	PCL6	PCL5	PCL4	PCL3	PCL2	PCL1	PCL0	PORTCL
$1006									Reserved
$1007	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	DDRC
$1008	0	0	PD5	PD4	PD3	PD2	PD1	PD0	PORTD
$1009	0	0	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	DDRD
$100A	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0	PORTE
$100B	FOC1	FOC2	FOC3	FOC4	FOC5	0	0	0	CFORC
$100C	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3	0	0	0	OC1M
$100D	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3	0	0	0	OC1D
$100E	Bit 15	14	13	12	11	10	9	Bit 8	TCNT (High)
$100F	Bit 7	6	5	4	3	2	1	Bit 0	TCNT (Low)
$1010	Bit 15	14	13	12	11	10	9	Bit 8	TIC1 (High)
$1011	Bit 7	6	5	4	3	2	1	Bit 0	TIC1 (Low)
$1012	Bit 15	14	13	12	11	10	9	Bit 8	TIC2 (High)
$1013	Bit 7	6	5	4	3	2	1	Bit 0	TIC2 (Low)
$1014	Bit 15	14	13	12	11	10	9	Bit 8	TIC3 (High)
$1015	Bit 7	6	5	4	3	2	1	Bit 0	TIC3 (Low)
$1016	Bit 15	14	13	12	11	10	9	Bit 8	TOC1(High)
$1017	Bit 7	6	5	4	3	2	1	Bit 0	TOC1 (Low)
$1018	Bit 15	14	13	12	11	10	9	Bit 8	TOC2 (High)
$1019	Bit 7	6	5	4	3	2	1	Bit 0	TOC2 (Low)
$101A	Bit 15	14	13	12	11	10	9	Bit 8	TOC3 (High)
$101B	Bit 7	6	5	4	3	2	1	Bit 0	TOC3 (Low)
$101C	Bit 15	14	13	12	11	10	9	Bit 8	TOC4 (High)
$101D	Bit 7	6	5	4	3	2	1	Bit 0	TOC4 (Low)
$101E	Bit 15	14	13	12	11	10	9	Bit 8	TI4O5 (High)
$101F	Bit 7	6	5	4	3	2	1	Bit 0	TI4O5 (Low)

Registers (2 of 2)

$1020	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5	TCTL1
$1021	EDG4B	EDG4A	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A	TCTL2
$1022	OC1I	OC2I	OC3I	OC4I	I4O5I	IC1I	IC2I	IC3I	TMSK1
$1023	OC1F	OC2F	OC3F	OC4F	I4O5F	IC1F	IC2F	IC3F	TFLG1
$1024	TOI	RTII	PAOVI	PAII	0	0	PR1	PR0	TMSK2
$1025	TOF	RTIF	PAOVF	PAIF	0	0	0	0	TFLG2
$1026	DDRA7	PAEN	PAMOD	PEDGE	DDRA3	I4/O5	RTR1	RTR0	PACTL
$1027	Bit 7	6	5	4	3	2	1	Bit 0	PACNT
$1028	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0	SPCR
$1029	SPIF	WCOL	0	MODF	0	0	0	0	SPSR
$102A	Bit 7	6	5	4	3	2	1	Bit 0	SPDR
$102B	TCLR	0	SCP1	SCP0	RCKB	SCR2	SCR1	SCR0	BAUD
$102C	R8	T8	0	M	WAKE	0	0	0	SCCR1
$102D	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	SCCR2
$102E	TDRE	TC	RDRF	IDLE	OR	NF	FE	0	SCSR
$102F	R7/T7	R6/T6	R5/T5	R4/T4	R3/T3	R2/T2	R1/T1	R0/T0	SCDR
$1030	CCF	0	SCAN	MULT	CD	CC	CB	CA	ADCTL
$1031	Bit 7	6	5	4	3	2	1	Bit 0	ADR1
$1032	Bit 7	6	5	4	3	2	1	Bit 0	ADR2
$1033	Bit 7	6	5	4	3	2	1	Bit 0	ADR3
$1034	Bit 7	6	5	4	3	2	1	Bit 0	ADR4
$1035	0	0	0	PTCON	BPRT3	BPRT2	BPRT1	BPRT0	BPROT
$1036–8									Reserved
$1039	ADPU	CSEL	IRQE	DLY	CME	0	CR1	CR0	OPTION
$103A	Bit 7	6	5	4	3	2	1	Bit 0	COPRST
$103B	ODD	EVEN	0	BYTE	ROW	ERASE	EELAT	EEPGM	PPROG
$103C	RBOOT	SMOD	MDA	IRV	PSEL3	PSEL2	PSEL1	PSEL0	HPRIO
$103D	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0	INIT
$103E	TILOP	0	OCCR	CBYP	DISR	FCM	FCOP	TCON	TEST1
$103F	EE3	EE2	EE1	EE0	1	NOCOP	1	EEON	CONFIG

HPRIO — Highest Priority I-Bit Interrupt and Miscellaneous **$103C**

	Bit 7	6	5	4	3	2	1	Bit 0
	RBOOT	SMOD	MDA	IRV	PSEL3	PSEL2	PSEL1	PSEL0
RESET:	—	—	—	—	0	1	0	1

RBOOT, SMOD, and MDA reset depend on power-up initialization mode and can only be written in special modes.

RBOOT — Read Bootstrap ROM

Set to one out of reset in bootstrap mode only

0 = Boot loader ROM disabled and not in map

1 = Boot loader ROM enabled and in map at $BF40–$BFFF

SMOD — Special Mode Select

MDA — Mode Select A

Inputs			Latched at Reset		
MODB	**MODA**	**Mode**	**RBOOT**	**SMOD**	**MDA**
1	0	Single-Chip	0	0	0
1	1	Expanded Multiplexed	0	0	1
0	0	Special Bootstrap	1	1	0
0	1	Special Test	0	1	1

IRV — Internal Read Visibility

0 = No internal read visibility on external bus

1 = Internal read data driven out data bus

For bits 3–0, refer to **Resets and Interrupts.**

INIT — RAM and I/O Mapping **$103D**

	Bit 7	6	5	4	3	2	1	Bit 0
	RAM3	RAM2	RAM1	RAM0	REG3	REG4	REG1	REG0
RESET:	0	0	0	0	0	0	0	1

RAM3–RAM0 — 512-Byte Internal RAM Map Position

RAM3–RAM0 determine the upper four bits of the RAM address, positioning RAM at the selected 4K boundary.

REG3–REG0 — 64-Byte Register Block Map Position

REG3–REG0 determine the upper four bits of the register address, positioning registers at the selected 4K boundary.

NOTE

Can be written only once in first 64 cycles out of reset in normal modes, or at any time in special modes. Refer to **Memory Maps** for more information.

TEST1 — Factory Test **$103E**

	Bit 7	6	5	4	3	2	1	Bit 0
	TILOP	0	OCCR	CBYP	DISR	FCM	FCOP	TCON
RESET:	0	0	0	0	—	0	0	0

Test modes only

TILOP — Test Illegal Opcode

OCCR — Output Condition Code Register to Timer Port

CBYP — Timer Divider Chain Bypass

DISR — Disable Resets from COP and Clock Monitor

DISR is forced to one out of reset in special test and bootstrap modes.

FCM — Force Clock Monitor Failure

FCOP — Force COP Watchdog Failure

TCON — Test Configuration Register

CONFIG — EEPROM Mapping and Enables, COP **$103F**

	Bit 7	6	5	4	3	2	1	Bit 0
	EE3	EE2	EE1	EE0	1	NOCOP	1	EEON
S. Chip or Boot:	1	1	1	1	1	P	1	1
RESET:	—	—	—	—	1	—	1	—
Expan. or Test:	P	P	P	P	1	P	1	P

NOTE

CONFIG is non-volatile and retains its previous programming even when the MCU has no power.

EE3–EE0 — EEPROM Map Position

EE3–EE0 determine the upper four bits of the EEPROM address, positioning EEPROM at the selected 4K boundary.

NOCOP — COP System Disable (Refer to **Resets and Interrupts**.)

EEON — EEPROM Enable

0 = 2K byte EEPROM is removed from the memory map
1 = 2K byte EEPROM is present in the memory map

Resets and Interrupts

The MC68HC811E2 has 3 reset vectors and 18 interrupt vectors. The reset vectors are:

- $\overline{\text{RESET}}$, or Power-On
- COP Clock Monitor Fail
- COP Failure

The 18 interrupt vectors service 23 interrupt sources (3 non-maskable, 20 maskable). The 3 non-maskable interrupt vectors are:

- Illegal Opcode Trap
- Software Interrupt
- $\overline{\text{XIRQ}}$ Pin (Pseudo Non-Maskable Interrupt)

The 20 interrupt sources are subject to masking by a global interrupt mask, the I bit in the CCR. In addition to the global I bit, all of these sources, except the external interrupt ($\overline{\text{IRQ}}$ pin), are controlled by local enable bits in control registers. Most interrupt sources in the M68HC11 have separate interrupt vectors, therefore there is usually no need for software to poll control registers to determine the cause of an interrupt. The maskable interrupt sources respond to a fixed-priority relationship, except that any one source can be dynamically elevated to the highest priority position of any maskable source. Refer to the table of interrupt and reset vector assignments.

On-chip peripheral systems generate maskable interrupts, which are recognized only if the global interrupt mask bit (I) in the condition code register (CCR) is clear. Maskable interrupts are prioritized according to a default arrangement, but any one source can be elevated to the highest maskable priority position by the HPRIO register. The HPRIO register can be written at any time, provided the I bit in the CCR is set.

Interrupt and Reset Vector Assignments

Vector Address	Interrupt Source	CC Register Mask	Local Mask
FFC0, C1 — FFD4, D5	Reserved	—	—
FFD6, D7	SCI Serial System	I Bit	
	• SCI Transmit Complete		TCIE
	• SCI Transmit Data Register Empty		TIE
	• SCI Idle Line Detect		ILIE
	• SCI Receiver Overrun		RIE
	• SCI Receive Data Register Full		RIE
FFD8, D9	SPI Serial Transfer Complete	I Bit	SPIE
FFDA, DB	Pulse Accumulator Input Edge	I Bit	PAII
FFDC, DD	Pulse Accumulator Overflow	I Bit	PAOVI
FFDE, DF	Timer Overflow	I Bit	TOI
FFE0, E1	Timer Input Capture 4/ Output Compare 5	I Bit	I4O5I
FFE3, E2	Timer Output Compare 4	I Bit	OC4I
FFE4, E5	Timer Output Compare 3	I Bit	OC3I
FFE6, E7	Timer Output Compare 2	I Bit	OC2I
FFE8, E9	Timer Output Compare 1	I Bit	OC1I
FFEA, EB	Timer Input Capture 3	I Bit	IC3
FFEC, ED	Timer Input Capture 2	I Bit	IC2I
FFEE, EF	Timer Input Capture 1	I Bit	IC1I
FFF0, F1	Real-Time Interrupt	I Bit	RTII
FFF2, F3	Parallel I/O Handshake	I Bit	STAI
	$\overline{\text{IRQ}}$ (External Pin)		None
FFF4, F5	$\overline{\text{XIRQ}}$ Pin	I Bit	None
FFF6, F7	Software Interrupt	None	None
FFF8, F9	Illegal Opcode Trap	None	None
FFFA, FB	COP Failure	None	NOCOP
FFFC, FD	Clock Monitor Fail	None	CME
FFFE, FF	$\overline{\text{RESET}}$	None	None

For some interrupt sources, such as the parallel I/O and SCI interrupts, the flags are automatically cleared during the normal course of responding to the interrupt requests. For example, the RDRF flag in the SCI system is cleared by the automatic clearing mechanism consisting of a read of the SCI status register while RDRF is set, followed by a read of the SCI data register. The normal response to an RDRF interrupt request is to read the SCI status register to check for receive errors, then to read the received data from the SCI data register. These two steps satisfy the automatic clearing mechanism without requiring any special instructions.

OPTION — System Configuration Options **$1039**

	Bit 7	6	5	4	3	2	1	Bit 0
	ADPU	CSEL	IRQE*	DLY*	CME	0	CR1*	CR0*
RESET:	0	0	0	1	0	0	0	0

*Can be written only once in first 64 cycles out of reset in normal modes, or at any time in special modes.

ADPU — A/D Power-Up (Refer to **Analog-to-Digital Converter.**)

CSEL — Clock Select (Refer to **Analog-to-Digital Converter.**)

IRQE — $\overline{IRQ}$ Select Edge Sensitive Only
- 0 = Low level recognition
- 1 = Falling edge recognition

DLY — Enable Oscillator Start-Up Delay on Exit from STOP
- 0 = No stabilization delay on exit from STOP
- 1 = Stabilization delay enabled on exit from STOP

CME — Clock Monitor Enable
- 0 = Clock monitor disabled; slow clocks can be used
- 1 = Slow or stopped clocks cause clock failure reset

CR1, CR0 — COP Timer Rate Select

CR [1:0]	Divide $E/2^{15}$ By	XTAL = 4.0 Mhz Timeout – 0/+32.8 ms	XTAL = 8.0 MHz Timeout – 0/+ 16.4 ms
0 0	1	32.768 ms	16.384 ms
0 1	4	131.072 ms	65.536 ms
1 0	16	524.288 ms	262.140 ms
1 1	64	2.097 sec	1.049 sec
	E =	1.0 MHz	2.0 MHz

COPRST — Arm/Reset COP Timer Circuitry **$103A**

	Bit 7	6	5	4	3	2	1	Bit 0
	7	6	5	4	3	2	1	0
RESET:	0	0	0	0	0	0	0	0

Write $55 to COPRST to arm COP watchdog clearing mechanism.
Write $AA to COPRST to reset COP watchdog.

HPRIO — Highest Priority I-Bit Interrupt and Miscellaneous **$103C**

	Bit 7	6	5	4	3	2	1	Bit 0
	RBOOT	SMOD	MDA	IRV	PSEL3	PSEL2	PSEL1	PSEL0
RESET:	—	—	—	—	0	1	0	1

For bits 7–4, refer to **Operating Modes.**

PSEL3–PSEL0 — Priority Select Bits 3–0

Writable only while the I bit in the CCR is set (interrupts disabled). These bits select one interrupt source to be elevated above all other I-bit related sources.

PSEL[3:0]	Interrupt Source Promoted
0 0 0 0	Timer Overflow
0 0 0 1	Pulse Accumulator Overflow
0 0 1 0	Pulse Accumulator Input Edge
0 0 1 1	SPI Serial Transfer Complete
0 1 0 0	SCI Serial System
0 1 0 1	Reserved (Default to $\overline{\text{IRQ}}$)
0 1 1 0	$\overline{\text{IRQ}}$ (External Pin or Parallel I/O)
0 1 1 1	Real-Time Interrupt
1 0 0 0	Timer Input Capture 1
1 0 0 1	Timer Input Capture 2
1 0 1 0	Timer Input Capture 3
1 0 1 1	Timer Output Compare 1
1 1 0 0	Timer Output Compare 2
1 1 0 1	Timer Output Compare 3
1 1 1 0	Timer Output Compare 4
1 1 1 1	Timer Output Compare 5/Input Capture 4

Electrically Erasable Programmable Read-Only Memory (EEPROM)

The EE3–EE0 bits in CONFIG control the position of the the 2K bytes of EEPROM in the memory map. In single chip and bootstrap modes, EE3–EE0 are forced to ones, positioning the EEPROM at $F800–$FFFF. In test mode, EEON is forced to zero to prevent interference between EEPROM and test accesses to memory.

An on-chip charge pump develops the high voltage required for programming and erasing. When the E clock is less than 1 MHz, select an internal clock to drive the EEPROM charge pump (write one to the CSEL bit in the OPTION register).

Programming and erasing the EEPROM is controlled by the PPROG register, depending on the block protect (BPROT) register value.

To erase the EEPROM, ensure that the proper bits of the BPROT register are cleared, then complete the following steps using the PPROG register:

1. Write to PPROG with the ERASE, EELAT, and appropriate BYTE and ROW bits set.
2. Write to the appropriate EEPROM address with any data ($x800–$x80F, $x810–$x81F through $xFF0–$xFFF). Row erase only requires a write to any location in the row. Bulk erase is accomplished by writing to any location in the array.
3. Write to PPROG with ERASE, EELAT, EEPGM, and the appropriate BYTE and ROW bits set.
4. Delay for 10 ms or more, as appropriate.
5. Clear the EEPGM bit in PPROG to turn off the high voltage.
6. Clear the PPROG register to reconfigure the EEPROM address and data buses for normal operation.

To program the EEPROM, ensure the proper bits of the BPROT register are cleared, then complete the following steps using the PPROG register:

1. Write to PPROG with the EELAT bit set.
2. Write data to the desired address.
3. Write to PPROG with the EELAT and EEPGM bits set.
4. Delay for 10 ms or more, as appropriate.
5. Clear the EEPGM bit in PPROG to turn off the high voltage.
6. Clear the PPROG register to reconfigure the EEPROM address and data buses for normal operation.

BPROT — Block Protect **$1035**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	0	PTCON	BPRT3	BPRT2	BPRT1	BPRT0
RESET:	0	0	0	1	1	1	1	1

NOTE

Block protect register bits can be written to zero, protection disabled within 64 cycles of a reset in normal modes, or at any time in special modes. Block protect register bits can be written to one, protection enabled, at any time.

PTCON — Protect for CONFIG

0 = CONFIG register can be programmed or erased normally.

1 = CONFIG register cannot be programmed or erased.

BPRT3–BPRT0 — Block Protect Bits for EEPROM

0 = Protection disabled for associated block

1 = Protection enabled for associated block

Bit Name	Block Protected	Block Size
BPRT0	$x800–$x9FF	512 Bytes
BPRT1	$xA00–$xBFF	512 Bytes
BPRT2	$xC00–$xDFF	512 Bytes
BPRT3	$xE00–$xFFF	512 Bytes

PPROG — EEPROM Programming Control **$103B**

	Bit 7	6	5	4	3	2	1	Bit 0
	ODD	EVEN	0	BYTE	ROW	ERASE	EELAT	EEPGM
RESET:	0	0	0	0	0	0	0	0

ODD — Program Odd Rows in Half of EEPROM (TEST)

EVEN — Program Even Rows in Half of EEPROM (TEST)

BYTE — Byte/Other EEPROM Erase Mode

ROW — Row/All EEPROM Erase Mode

BYTE	ROW	Action
0	0	Bulk Erase (All 2K Bytes)
0	1	Row Erase (16 Bytes)
1	0	Byte Erase
1	1	Byte Erase

ERASE — Erase/Normal Control for EEPROM

0 = Normal read or program mode

1 = Erase mode

EELAT — EEPROM Latch Control

0 = EEPROM address and data bus configured for normal reads

1 = EEPROM address and data bus configured for programming or erasing

EEPGM — EEPROM Program Command

0 = Programming or erase voltage switched off to EEPROM array

1 = Programming or erase voltage switched on to EEPROM array

CONFIG — EEPROM Mapping and Enables, COP **$103F**

	Bit 7	6	5	4	3	2	1	Bit 0
	EE3	EE2	EE1	EE0	1	NOCOP	1	EEON
S. Chip or Boot:	1	1	1	1	1	P	1	1
RESET:	—	—	—	—	1	—	1	—
Expan. or Test:	P	P	P	P	1	P	1	P

NOTE

CONFIG is non-volatile and retains its previous programming, even when the MCU has no power.

EE3–EE0 — EEPROM Map Position

EE3–EE0 determine the upper four bits of the EEPROM address, positioning EEPROM at the selected 4K boundary.

NOCOP — COP System Disable (Refer to **Resets and Interrupts.**)

EEON — EEPROM Enable

0 = 2K-byte EEPROM is removed from the memory map

1 = 2K-byte EEPROM is present in the memory map

Parallel Input/Output

The MC68HC811E2 has 5 I/O ports, configurable with up to 38 input/output lines, depending on the operating mode. The following table summarizes the ports and their shared functions:

Port	Input Pins	Output Pins	Bidirectional Pins	Shared Functions
Port A	3	4	1	Timer
Port B	—	8	—	High Order Address
Port C	—	—	8	Low Order Address & Data bus
Port D	—	—	6	SCI & SPI
Port E	8	—	—	A/D Converter

Parallel I/O Handshake

Simple and full handshake input and output functions are available on ports B and C lines in single-chip mode. The following is a description of the handshake functions.

In simple strobed mode, port B is a strobed output port, and port C is a latching input port. The two activities are available simultaneously.

The STRB output is pulsed for two E-clock periods each time there is a write to the PORTB register. The INVB bit in the PIOC register controls the polarity of STRB pulses. Port C levels are latched into the alternate port C latch (PORTCL) register on each assertion of the STRA input. STRA edge select, flag, and interrupt enable bits are located in the PIOC register. Any or all of the port C lines can be used as general-purpose I/O while in strobed input mode.

Full handshake modes involve port C pins and the STRA and STRB lines. Input and output handshake modes are supported, and output handshake mode has a three-stated variation. STRA is an edge detecting input and STRB is a handshake output. Control and enable bits are located in the PIOC register.

In full input handshake mode, the MCU uses STRB as a **ready** line to an external system. Port C logic levels are latched into PORTCL when the STRA line is asserted by the external system. The MCU then deasserts STRB. The MCU reasserts STRB after the PORTCL register is read. A mix of latched inputs, static inputs, and static outputs is allowed on port C, differentiated by the data direction bits and use of the PORTC and PORTCL registers.

In full output handshake mode, the MCU writes data to PORTCL, which, in turn, asserts the STRB output to indicate that data is ready. The external system reads port C and asserts the STRA input to acknowledge that data has been received.

In the three-state variation of output handshake mode, lines intended as three-state handshake outputs are configured as inputs by clearing the corresponding DDRC bits. The MCU writes data to PORTCL and asserts STRB. The external system responds by activating the STRA input, which forces the MCU to drive the data in PORTCL out on all of the port C lines. The mode variation does not allow part of port C to be used for static inputs while other port C pins are being used for handshake outputs. Refer to the PIOC register description.

PORTA — Port A Data **$1000**

	Bit 7	6	5	4	3	2	1	Bit 0
	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
RESET:	HiZ	0	0	0	HiZ	HiZ	HiZ	HiZ
Alt. Pin Func.:	PAI	OC2	OC3	OC4	OC5/IC4	IC1	IC2	IC3
And/or:	OC1	OC1	OC1	OC1	OC1	—	—	—

PIOC — Parallel I/O Control $1002

	Bit 7	6	5	4	3	2	1	Bit 0
	STAF	STAI	CWOM	HNDS	OIN	PLS	EGA	INVB
RESET:	0	0	0	0	0	U	1	1

STAF — Strobe A Interrupt Status Flag

Set when selected edge occurs on Strobe A

Cleared by PIOC read with STAF set followed by PORTCL read (simple strobed or full input handshake mode) or PORTCL write (output handshake mode)

STAI — Strobe A Interrupt Enable Mask

0 = STAF interrupts disabled
1 = STAF interrupts enabled

CWOM — Port C Wire-OR Mode (affects all eight port C pins)

0 = Port C outputs are normal CMOS outputs
1 = Port C outputs are open-drain outputs

HNDS — Handshake Mode

0 = Simple strobe mode
1 = Full input or output handshake mode

OIN — Output or Input Handshake Select

HNDS must be set to one for this bit to have meaning.

0 = Input handshake
1 = Output handshake

PLS — Pulse/Interlocked Handshake Operation

HNDS must be set to one for this bit to have meaning. Once activated, strobe B stays active until the selected edge of strobe A is detected.

0 = Interlocked handshake
1 = Pulsed handshake (Strobe B pulses high for 2 E-clock cycles)

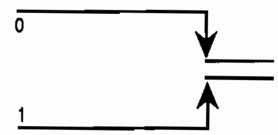
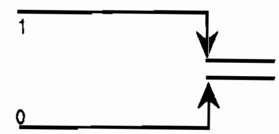
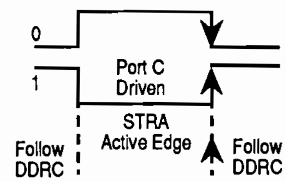
EGA — Active Edge for Strobe A

0 = STRA falling edge selected
1 = STRA rising edge selected

INVB — Invert Strobe B

0 = Active level is logic zero
1 = Active level is logic one

Parallel I/O Control

	STAF Clearing Sequence	HNDS	OIN	PLS	EGA	Port C	Port B
Simple strobed mode	Read PIOC with STAF=1 then read PORTCL	0	X	X		Inputs latched into PORTCL on any active edge on STRA	STRB pulses on writes to port B
Full input handshake	Read PIOC with STAF=1 then read PORTCL	1	0	0 = STRB active level 1 = STRB active pulse		Inputs latched into PORTCL on any active edge on STRA	Normal output port, unaffected in handshake modes
Full output handshake	Read PIOC with STAF=1 then write to PORTCL	1	1	0 = STRB active level 1 = STRB active pulse		Driven as outputs if STRA at active level, follows DDRC if STRA not at active level	Normal output port, unaffected in handshake modes

PORTC — Port C Data **$1003**

	Bit 7	6	5	4	3	2	1	Bit 0
	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
S. Chip or Boot:	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
RESET:	0	0	0	0	0	0	0	0
Expan. or Test:	A7/D7	A6/D6	A5/D5	A4/D4	A3/D3	A2/D2	A1/D1	A0/D0

NOTE

In single chip and boot modes, port C pins reset to high-impedance inputs (DDRC registers are set to zero). In expanded and special test modes, port C pins are multiplexed address/data bus and the port C register address is treated as an external memory location.

PORTB — Port B Data $1004

	Bit 7	6	5	4	3	2	1	Bit 0
	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
S. Chip or Boot:	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
RESET:	0	0	0	0	0	0	0	0
Expan. or Test:	A15	A14	A13	A12	A11	A10	A9	A8

PORTCL — Port C Latched $1005

	Bit 7	6	5	4	3	2	1	Bit 0
	PCL7	PCL6	PCL5	PCL4	PCL3	PCL2	PCL1	PCL0
RESET:	U	U	U	U	U	U	U	U

Writes affect port C pins. PORTCL is used in the handshake clearing mechanism.
When an active edge occurs on the STRA pin, port C data is latched into the PORTCL register.

DDRC — Data Direction Register for Port C $1007

	Bit 7	6	5	4	3	2	1	Bit 0
	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0
RESET:	0	0	0	0	0	0	0	0

DDC7–DDC0 — Data Direction for Port C

0 = Input

1 = Output

PORTD — Port D Data $1008

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	PD5	PD4	PD3	PD2	PD1	PD0
RESET:	0	0	0	0	0	0	0	0
Alt. Pin Func.:	—	—	$\overline{SS}$	SCK	MOSI	MISO	TxD	RxD

DDRD — Data Direction Register for Port D **$1009**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0
RESET:	0	0	0	0	0	0	0	0
Alt. Pin Func.:	—	—	PD5/ $\overline{SS}$	PD4/ SCK	PD3/ MOSI	PD2/ MISO	PD1/ TxD	PD0/ RxD

DDD5–DDD0 — Data Direction for Port D

When DDRD bit 5 is zero and MSTR = 1 in SPCR, PD5/$\overline{SS}$ is a general-purpose output and mode fault logic is disabled.

0 = Input

1 = Output

PORTE — Port E Data **$100A**

	Bit 7	6	5	4	3	2	1	Bit 0
	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
RESET:	U	U	U	U	U	U	U	U
Alt. Pin Func.:	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0

PACTL — Pulse Accumulator Control **$1026**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDRA7	PAEN	PAMOD	PEDGE	DDRA3	I4/O5	RTR1	RTR0
RESET:	0	0	0	0	0	0	0	0

For bits 6–4, refer to **Pulse Accumulator**. For bits 1 and 0, refer to **Main Timer.**

DDRA7 — Data Direction for Port A Bit 7

0 = Input only

1 = Output

DDRA3 — Data Direction for Port A Bit 3

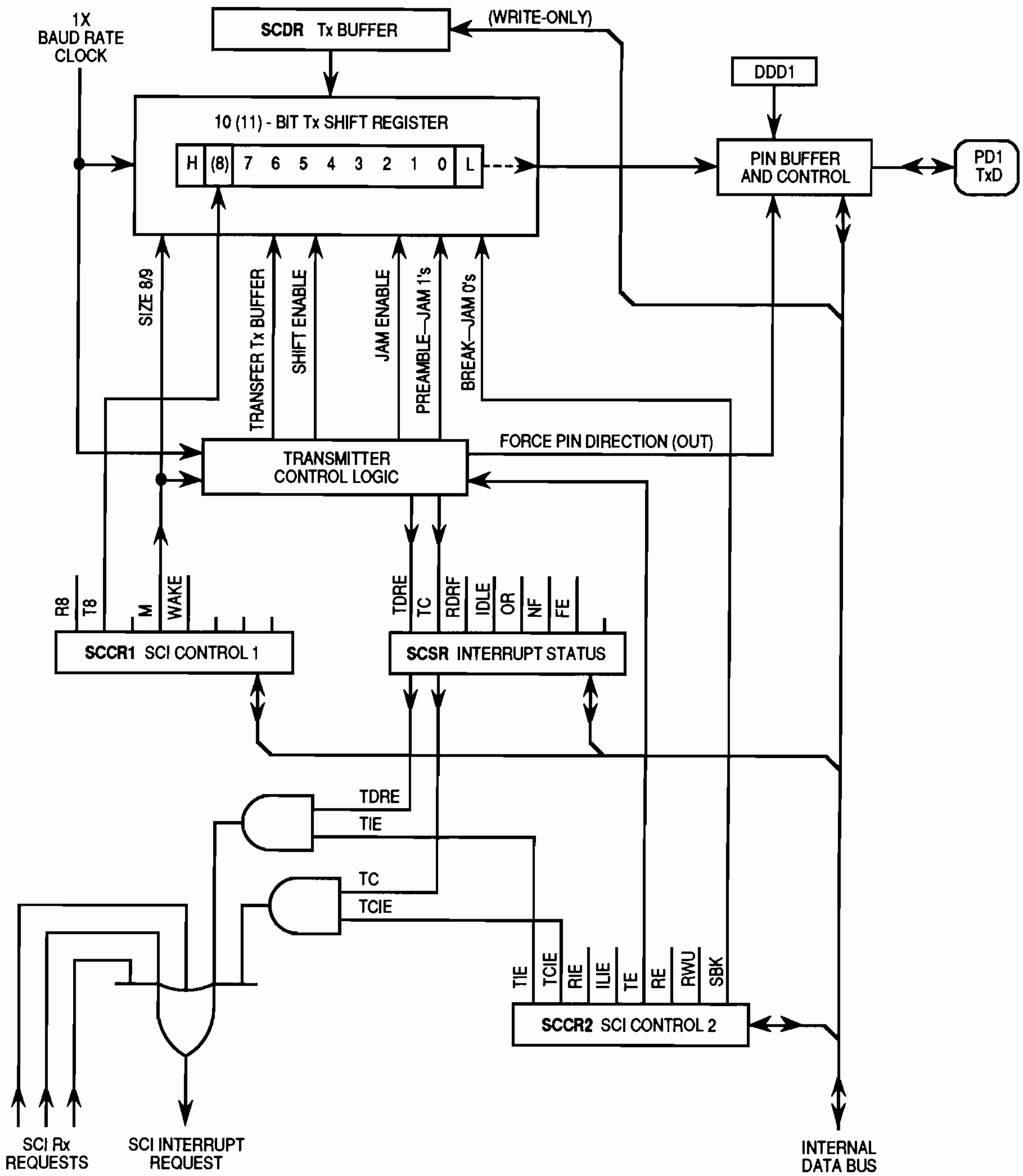
Overridden if an output compare function is configured to control the PA3 pin.

0 = Input

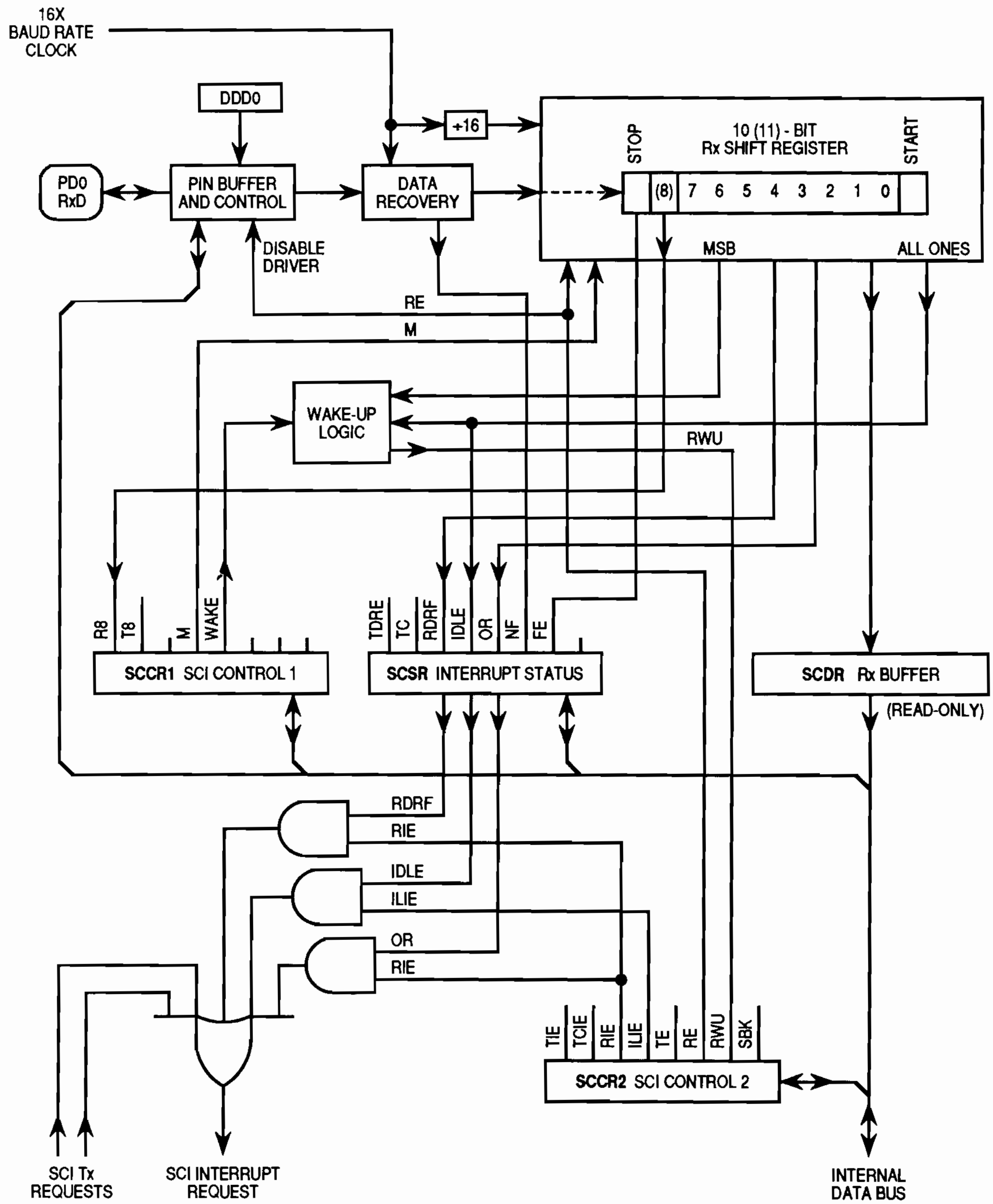
1 = Output

Serial Communications Interface (SCI)

The SCI is a universal asynchronous receiver transmitter (UART) serial communications interface, one of two independent serial I/O subsystems in the MC68HC811E2. It has a standard NRZ format (one start, eight or nine data and one stop bit), and several baud rates available. The SCI transmitter and receiver are independent, but use the same data format and bit rate.



SCI Transmitter Block Diagram



SCI Receiver Block Diagram

SPCR — Serial Peripheral Control $1028

	Bit 7	6	5	4	3	2	1	Bit 0
	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0
RESET:	0	0	0	0	0	1	U	U

For bits 7 and 6 and bits 4–0, refer to **SPI** section.

DWOM — Port D Wired-OR Mode

DWOM affects all six port D pins

0 = Normal CMOS outputs

1 = Open-drain outputs

BAUD — Baud Rate $102B

	Bit 7	6	5	4	3	2	1	Bit 0
	TCLR	0	SCP1	SCP0	RCKB	SCR2	SCR1	SCR0
RESET:	0	0	0	0	0	U	U	U

TCLR — Clear Baud Rate Counters (TEST)

RCKB — SCI Baud Rate Clock Check (TEST)

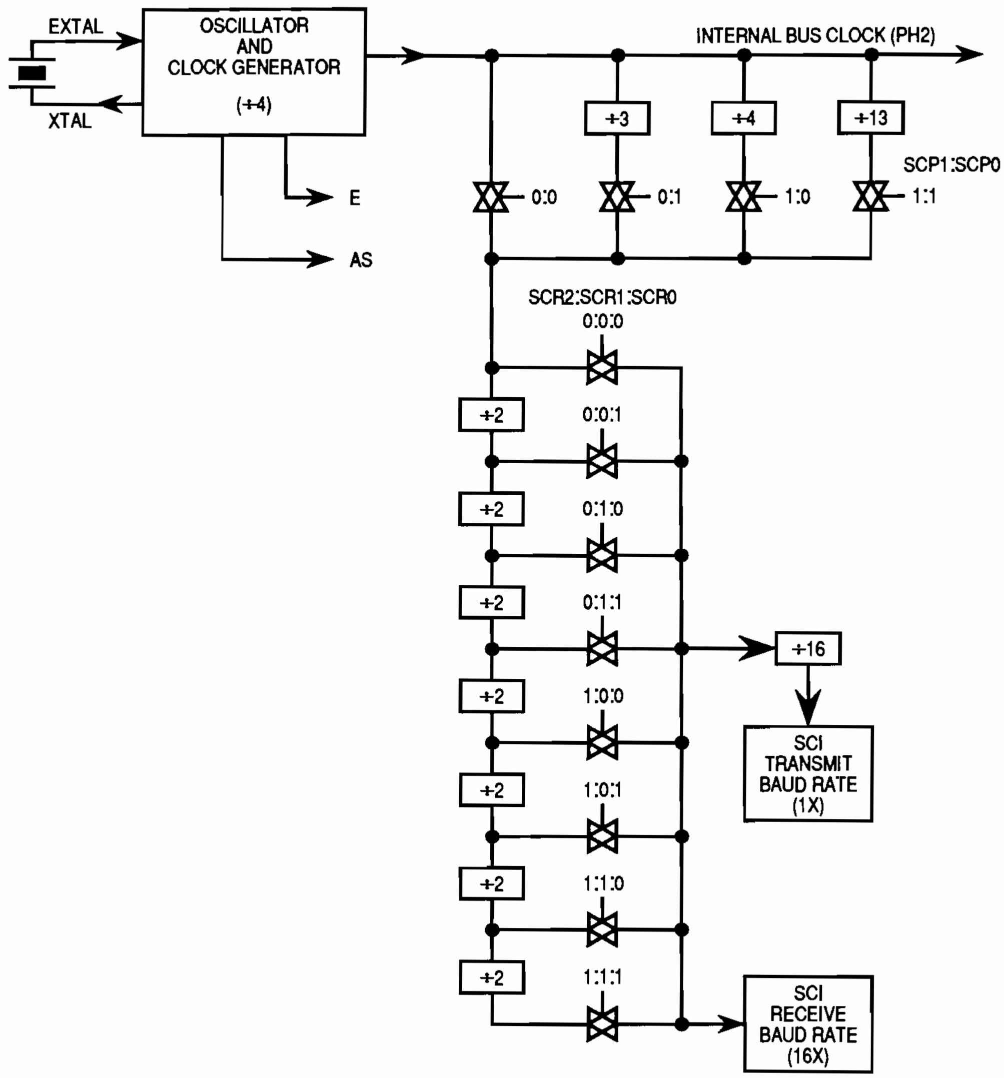
SCP1, SCP0 — SCI Baud Rate Prescaler Selects

SCP [1:0]	Divide Internal Clock By	Crystal Frequency in MHz 4.0 MHz (Baud)	8.0 MHz (Baud)
0 0	1	62.50K	125.0K
0 1	3	20.83K	41.67K
1 0	4	15.625K	31.25K
1 1	13	4800	9600

SCR2, SCR1, and SCR0 — SCI Baud Rate Selects

Selects receiver and transmitter bit rate based on output from baud rate prescaler stage.

SCR [2:0]	Divide Prescaler By	Highest Baud Rate (Prescaler Output from Previous Table) 4800	9600
0 0 0	1	4800	9600
0 0 1	2	2400	4800
0 1 0	4	1200	2400
0 1 1	8	600	1200
1 0 0	16	300	600
1 0 1	32	150	300
1 1 0	64	—	150
1 1 1	128	—	—



SCI Baud Rate Diagram

SCCR1 — SCI Control 1 **$002C**

	Bit 7	6	5	4	3	2	1	Bit 0
	R8	T8	0	M	WAKE	0	0	0
RESET:	U	U	0	0	0	0	0	0

R8 — Receive Data Bit 8

If M bit is set, R8 stores ninth bit in receive data character.

T8 — Transmit Data Bit 8

If M bit is set, T8 stores ninth bit in transmit data character.

M — Mode (Select Character Format)
0 = Start, 8 data bits, 1 stop bit
1 = Start, 9 data bits, 1 stop bit

WAKE — Wake Up by Address Mark/Idle
0 = Wake up by IDLE line recognition
1 = Wake up by address mark (most significant bit set)

SCCR2 — SCI Control 2 **$102D**

	Bit 7	6	5	4	3	2	1	Bit 0
	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
RESET:	0	0	0	0	0	0	0	0

TIE — Transmit Interrupt Enable
0 = TDRE interrupts disabled
1 = SCI interrupt requested when TRE status flag is set

TCIE — Transmit Complete Interrupt Enable
0 = TC interrupts disabled
1 = SCI interrupt requested when TC status flag is set

RIE — Receiver Interrupt Enable
0 = RDRF and OR interrupts disabled
1 = SCI interrupt requested when RDRF flag or the OR status flag is set

ILIE — Idle Line Interrupt Enable
0 = IDLE interrupts disabled
1 = SCI interrupt requested when IDLE status flag is set

TE — Transmitter Enable
0 = Transmitter disabled
1 = Transmitter enabled

RE — Receiver Enable
0 = Receiver disabled
1 = Receiver enabled

RWU — Receiver Wake-Up Control
0 = Normal SCI receiver
1 = Wake-up enabled and receiver interrupts inhibited

SBK — Send Break
0 = Break generator off
1 = Break codes generate as long as SBK = 1

SCSR — SCI Status **$102E**

	Bit 7	6	5	4	3	2	1	Bit 0
	TDRE	TC	RDRF	ILE	OR	NF	FE	0
RESET:	1	1	0	0	0	0	0	0

TDRE — Transmit Data Register Empty Flag
Set if transmit data can be written to SCDR; if TDRE = 0, transmit data register is busy
Cleared by SCSR read with TDRE set, followed by SCDR write

TC — Transmit Complete Flag
Set if transmitter is idle (no data, preamble, or break transmission in progress)
Cleared by SCSR read with TC set, followed by SCDR write

RDRF — Receive Data Register Full Flag
Set if a received character is ready to be read from SCDR
Cleared by SCSR read with RDRF set, followed by SCDR read

IDLE — Idle Line Detected Flag
Set if the RxD line is idle. When RWU = 1, IDLE flag is inhibited
Cleared by SCSR read with IDLE set, followed by SCDR read
Once cleared, IDLE is not set again until the RxD line has been active and becomes idle again

OR — Overrun Error Flag
Set if a new character is received before a previously received character is read from SCDR
Cleared by SCSR read with OR set, followed by SCDR read

NF — Noise Error Flag
Set if majority sample logic detects anything other than a unanimous decision
Cleared by SCSR read with NF set, followed by SCDR read

FE — Framing Error
Set if a 0 is detected where a stop bit was expected
Cleared by SCSR read with FE set, followed by SCDR read

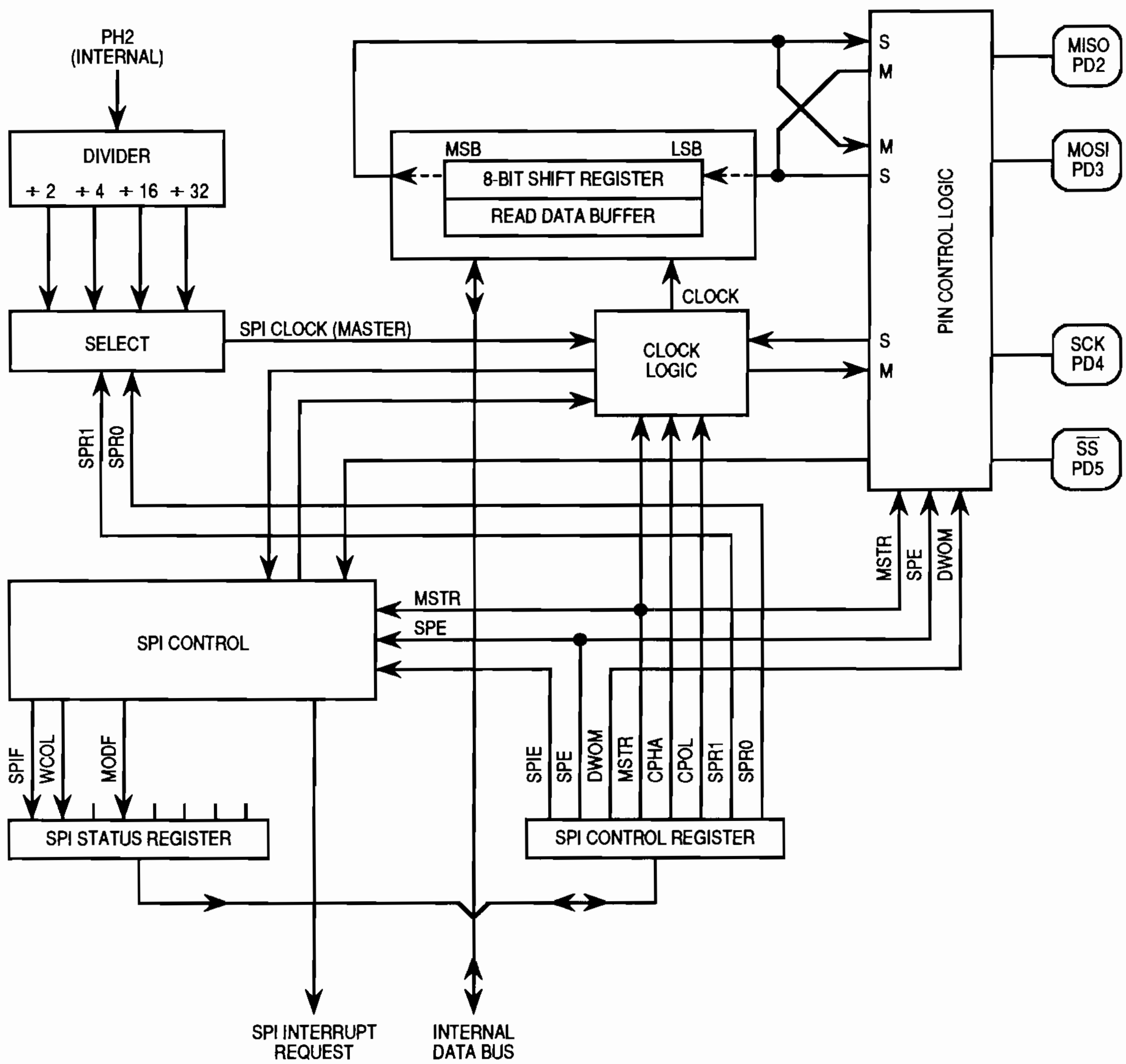
SCDR — SCI Data **$102F**

	Bit 7	6	5	4	3	2	1	Bit 0
	R7/T7	R6/T6	R5/T5	R4/T4	R3/T3	R2/T2	R1/T1	R0/T0
RESET:	U	U	U	U	U	U	U	U

Receive and transmit are double buffered. Reads access the receive data buffer, and writes access the transmit data buffer.

Serial Peripheral Interface (SPI)

The SPI is one of two independent serial communications subsystems that allows the MCU to communicate synchronously with peripheral devices and other microprocessors. Data rates can be as high as one half of the E clock rate when configured as master and as fast as the E clock when configured as slave.



SPI Block Diagram

DDRD — Data Direction Register for Port D **$1009**

	Bit 7	6	5	4	3	2	1	Bit 0
	0	0	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0
RESET:	0	0	0	0	0	0	0	0
Alt. Pin Func.:	—	—	PD5/ $\overline{SS}$	PD4/ SCK	PD3/ MOSI	PD2/ MISO	PD1/ TxD	PD0/ RxD

DDD5–DDD0 — Data Direction for Port D

When DDRD bit 5 is zero and MSTR = 1 in SPCR, PD5/$\overline{SS}$ is a general-purpose output and mode fault logic is disabled.

0 = Input

1 = Output

SPCR — Serial Peripheral Control **$1028**

	Bit 7	6	5	4	3	2	1	Bit 0
	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0
RESET:	0	0	0	0	0	1	U	U

SPIE — Serial Peripheral Interrupt Enable

0 = SPI interrupts disabled

1 = SPI interrupts enabled

SPE — Serial Peripheral System Enable

0 = SPI off

1 = SPI on

DWOM — Port D Wire-OR Mode

DWOM effects all six port D pins

0 = Normal CMOS outputs

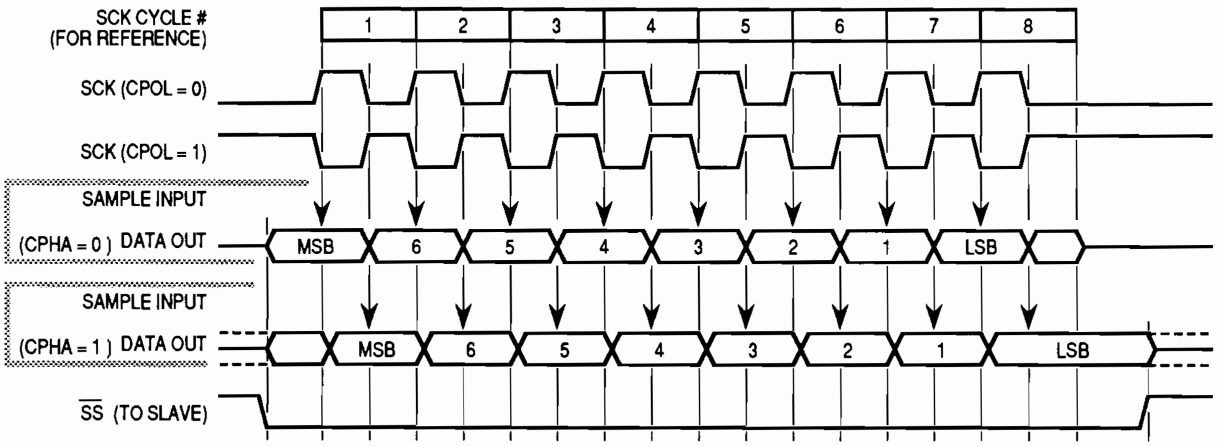
1 = Open-drain outputs

MSTR — Master Mode Select

0 = Slave mode

1 = Master mode

CPOL, CPHA — Clock Polarity, Clock Phase (Refer to **SPI Transfer Format** figure.)



NOTE: This figure shows the LSBF = 0 default case. If LSBF = 1, data is transferred in reverse order (LSB first).

SPI Transfer Format

SPR1 and SPR0 — SPI Clock Rate Selects

SPI Clock Rate Selects

SPR [1:0]	E Clock Divide By	Frequency at E = 1 MHz (Baud)	Frequency at E = 2 MHz (Baud)
0 0	2	500 kHz	1.0 MHz
0 1	4	250 kHz	500 kHz
1 0	16	62.5 kHz	125 kHz
1 1	32	31.25 kHz	62.5 kHz

SPSR — Serial Peripheral Status **$1029**

	Bit 7	6	5	4	3	2	1	Bit 0
	SPIF	WCOL	0	MODF	0	0	0	0
RESET:	0	0	0	0	0	0	0	0

SPIF — SPI Transfer Complete Flag

Set when and SPI transfer is complete.

Cleared by reading SPSR with SPIF set, followed by SPR access.

WCOL — Write Collision

Set when SPDR is written while transfer is in progress.

Cleared by SPSR with WCOL set, followed by SPR access.

MODF — Mode Fault (A Mode Fault Terminates SPI Operation)

Set when $\overline{SS}$ is pulled low while MSTR = 1.

Cleared by SPSR read with MODF set, followed by SPCR write.

SPDR — SPI Data **$102A**

Bit 7	6	5	4	3	2	1	Bit 0
Bit 7	6	5	4	3	2	1	Bit 0

SPI is double buffered in, single buffered out.

Main Timer

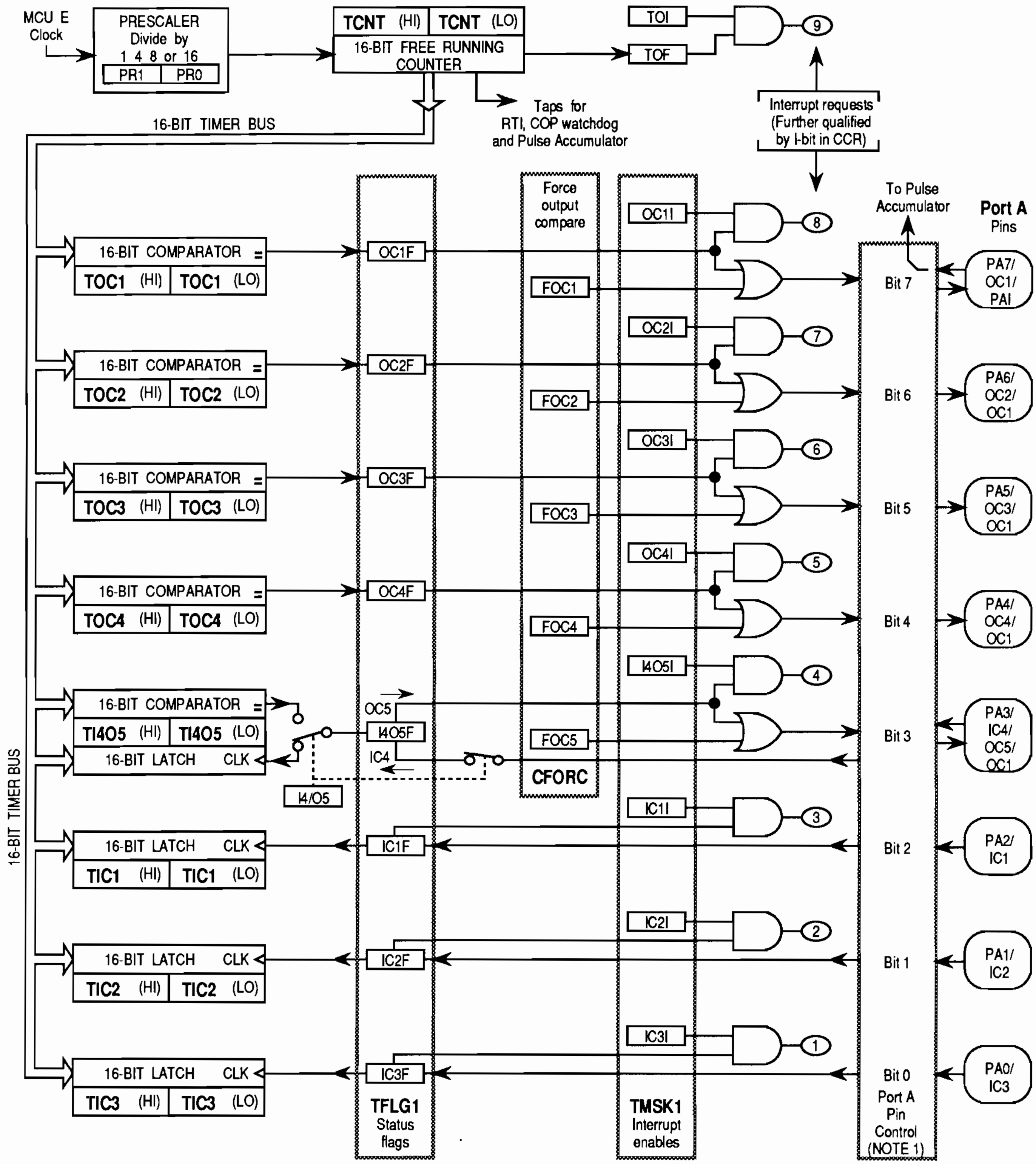
The main timer is based on a free-running 16-bit counter with a four-stage programmable prescaler. A timer overflow function allows software to extend the system's timing capability beyond the counter's16-bit range.

The timer has three channels of input capture, four channels of output compare, and one channel that can be configured as a fourth input capture or a fifth output compare.

The following table summarizes crystal-related frequencies and periods.

Timer Summary

Control Bits	XTAL Frequencies		
	4.0 MHz	8.0 MHz	Other Rates
	1.0 MHz	2.0 MHz	(E)
	1000 ns	500 ns	(1/E)
PR [1:0]	**Main Timer Count Rates**		
0 0 1 count — overflow —	1.0 µs 65.536 ms	500 ns 32.768 ms	(E/1) ($E/2^{16}$)
0 1 1 count — overflow —	4.0 µs 262.14 ms	2.0 µs 131.07 ms	(E/4) ($E/2^{18}$)
1 0 1 count — overflow —	8.0 µs 524.29 ms	4.0 µs 262.14 ms	(E/8) ($E/2^{19}$)
1 1 1 count — overflow —	16.0 µs 1.049 s	8.0 µs 524.29 ms	(E/16) ($E/2^{20}$)
RTR [1:0]	**Periodic (RTI) Interrupt Rates**		
0 0 0 1 1 0 1 1	8.192 ms 16.384 ms 32.768 ms 65.536 ms	4.096 ms 8.192 ms 16.384 ms 32.768 ms	($E/2^{13}$) ($E/2^{14}$) ($E/2^{15}$) ($E/2^{16}$)



Main Timer

Note: Port A pin actions are controlled by OC1M, OC1D, PACTL, TCTL1, and TCTL2 registers.

CFORC — Timer Compare Force $100B

	Bit 7	6	5	4	3	2	1	Bit 0
	FOC1	FOC2	FOC3	FOC4	FOC5	0	0	0
RESET:	0	0	0	0	0	0	0	0

FOC5–FOC1 — Write ones to Force Compare(s)
0 = Not affected
1 = Output compare x action occurs

OC1M — Output Compare 1 Mask $100C

	Bit 7	6	5	4	3	2	1	Bit 0
	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3	0	0	0
RESET:	0	0	0	0	0	0	0	0

Set bit(s) to enable OC1 to control corresponding pin(s) of port A.

OC1D — Output Compare 1 Data $100D

	Bit 7	6	5	4	3	2	1	Bit 0
	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3	0	0	0
RESET:	0	0	0	0	0	0	0	0

If OC1Mx is set, data in OC1Dx is output to port A bit x on successful OC1 compares.

TCNT — Timer Count $100E, $100F

$100E	Bit 15	14	13	12	11	10	9	Bit 8	High	**TCNT**
$100F	Bit 7	6	5	4	3	2	1	Bit 0	Low	

TCNT resets to $0000.
In normal modes, TCNT is read-only.

TIC1–TIC3 — Timer Input Capture $1010–$1015

$1010	Bit 15	14	13	12	11	10	9	Bit 8	High	TIC1
$1011	Bit 7	6	5	4	3	2	1	Bit 0	Low	
$1012	Bit 15	14	13	12	11	10	9	Bit 8	High	TIC2
$1013	Bit 7	6	5	4	3	2	1	Bit 0	Low	
$1014	Bit 15	14	13	12	11	10	9	Bit 8	High	TIC3
$1015	Bit 7	6	5	4	3	2	1	Bit 0	Low	

TICx not affected by reset

TOC1–TOC4 — Timer Output Compare $1016–$101D

$1016	Bit 15	14	13	12	11	10	9	Bit 8	High	TOC1
$1017	Bit 7	6	5	4	3	2	1	Bit 0	Low	
$1018	Bit 15	14	13	12	11	10	9	Bit 8	High	TOC2
$1019	Bit 7	6	5	4	3	2	1	Bi -0	Low	
$101A	Bit 15	14	13	12	11	10	9	Bi -8	High	TOC3
$101B	Bit 7	6	5	4	3	2	1	Bit 0	Low	
$101C	Bit 15	14	13	12	11	10	9	Bit 8	High	TOC4
$101D	Bit 7	6	5	4	3	2	1	Bit 0	Low	
$101E	Bit 15	14	13	12	11	10	9	Bit 8	High	TOC5
$101F	Bit 7	6	5	4	3	2	1	Bit 0	Low	

All TOCx register pairs reset to ones ($FFFF)

TI4O5 — Timer Input Capture 4/Output Compare 5 $101E, $101F

$101E	Bit 15	14	13	12	11	10	9	Bit 8	High	TI4O5
$101F	Bit 7	6	5	4	3	2	1	Bit 0	Low	

All TI4O5 register pairs reset to ones ($FFFF).

TCTL1 — Timer Control 1 **$1020**

	Bit 7	6	5	4	3	2	1	Bit 0
	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5
RESET:	0	0	0	0	0	0	0	0

OM2–OM5 — Output Mode

OL2–OL5 — Output Level

OMx	OLx	Action Taken on Successful Compare
0	0	Timer disconnected from output pin logic.
0	1	Toggle OCx output line.
1	0	Clear OCx output line to 0.
1	1	Set OCx output line to 1.

TCTL2 — Timer Control 2 **$1021**

	Bit 7	6	5	4	3	2	1	Bit 0
	EDG4B	EDG4A	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A
RESET:	0	0	0	0	0	0	0	0

Timer Control Configuration

EDGxB	EDGxA	Configuration
0	0	Capture disabled
0	1	Capture on rising edges only
1	0	Capture on falling edges only
1	1	Capture on any edge

TMSK1 — Timer Interrupt Mask 1 **$1022**

	Bit 7	6	5	4	3	2	1	Bit 0
	OC1I	OC2I	OC3I	OC4I	I4O5I	IC1I	IC2I	IC3I
RESET:	0	0	0	0	0	0	0	0

OC1I–OC4I — Output Compare x Interrupt Enable
If the OCxI enable bit is set when the OCxF flag bit is set, a hardware interrupt sequence is requested.

I4O5I — Input Capture 4 or Output Compare 5 Interrupt Enable
When I4/O5 in PACTL is one, I4O5I is the input capture 4 interrupt bit.
When I4/O5 in PACTL is zero, I4O5I is the output compare 5 interrupt control bit.

IC1I–IC3I — Input Capture x Interrupt Enable
If the ICxI enable bit is set when the ICxF flag bit is set, a hardware interrupt sequence is requested.

NOTE

Bits in TMSK1 correspond bit for bit with flag bits in TFLG1. Ones in TMSK1 enable the corresponding interrupt sources.

TFLG1 — Timer Interrupt Flag 1 **$1023**

	Bit 7	6	5	4	3	2	1	Bit 0
	OC1F	OC2F	OC3F	OC4F	I4O5F	IC1F	IC2F	IC3F
RESET:	0	0	0	0	0	0	0	0

Clear flags by writing a one to the corresponding bit position(s).

OC1F–OC4F — Output Compare x Flag
Set each time the counter matches output compare x value.

I4O5F — Input Capture 4/Output Compare 5 Flag
Set by IC4 or OC5, depending on which function was enabled by I4O5 bit in PACTL.

IC1F–IC3F — Input Capture x Flag
Set each time a selected active edge is detected on the ICx input line.

TMSK2 — Timer Interrupt Mask 2 **$1024**

	Bit 7	6	5	4	3	2	1	Bit 0
	TOI	RTII	PAOVI	PAII	0	0	PR1	PR0
RESET:	0	0	0	0	0	0	0	0

TOI — Timer Overflow Interrupt Enable
0 = TOF interrupts disabled
1 = Interrupt requested when TOF is set to one

RTII — Real-Time Interrupt Enable
0 = RTIF interrupts disabled
1 = Interrupt requested when RTIF is set to one

For bits 5 and 4, refer to **Pulse Accumulator.**

NOTE

Bits in TMSK2 correspond bit for bit with flag bits in TFLG2. Ones in TMSK2 enable the corresponding interrupt sources.

PR1 and PR0 — Timer Prescaler Select

In normal modes, PR1 and PR0 may only be written once, and the write must be within 64 cycles after reset. (Refer to **Timer Summary** table for specific timing values.)

PR [1:0]	Prescaler
0 0	1
0 1	4
1 0	8
1 1	16

TFLG2 — Timer Interrupt Flag 2 **$1025**

	Bit 7	6	5	4	3	2	1	Bit 0
	TOF	RTIF	PAOVF	PAIF	0	0	0	0
RESET:	0	0	0	0	0	0	0	0

Clear flags by writing a one to the corresponding bit position(s).

TOF — Timer Overflow Flag

Set when TCNT changes from $FFFF to $0000.

RTIF — Real Time (Periodic) Interrupt Flag

Set periodically (Refer to **Main Timer.**)

For bits 6 and 5, refer to **Pulse Accumulator**.

PACTL — Pulse Accumulator Control **$1026**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDRA7	PAEN	PAMOD	PEDGE	DDRA3	I4/O5	RTR1	RTR0
RESET:	0	0	0	0	0	0	0	0

For bits 7 and 3, refer to **Parallel I/O**.

For bits 6–4, refer to **Pulse Accumulator.**

I4/O5 — Input Capture 4/Output Compare 5

0 = OC5 enabled

1 = IC4 enabled

RTR1 and RTR0 — Real-Time Interrupt (RTI) Rate

Real-Time Interrupt Rates

RTR [1:0]	Divide E By	XTAL = 4.0 MHz	XTAL = 8.0 MHz
0 0	2^{13}	8.19 ms	4.096 ms
0 1	2^{14}	16.38 ms	8.192 ms
1 0	2^{15}	32.77 ms	16.384 ms
1 1	2^{16}	65.54 ms	32.768 ms
	E =	1.0 MHz	2.0 MHz

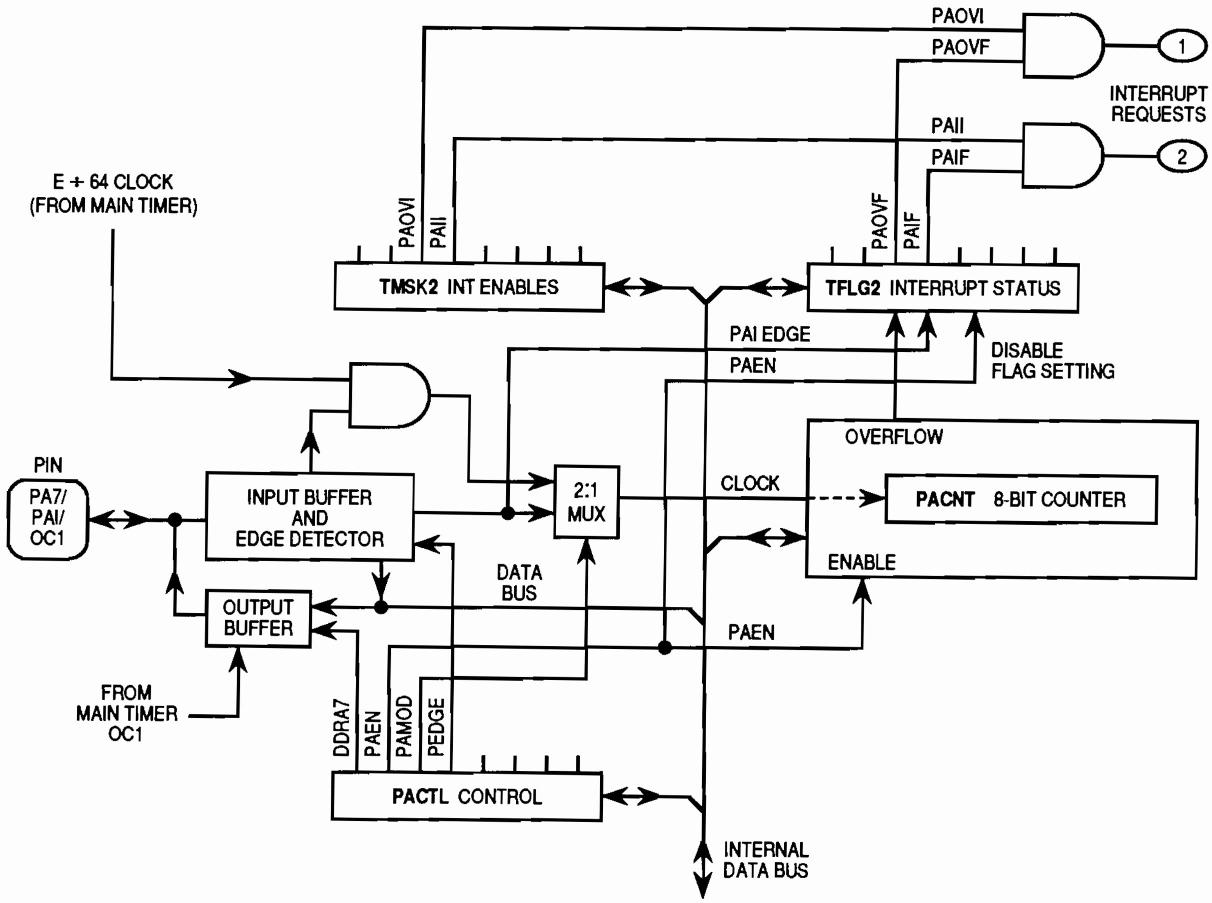
Pulse Accumulator

The MC68HC811E2 has an 8-bit counter that can be configured to operate as a simple event counter or for gated time accumulation, depending on the PAMOD bit in the PACTL register. The pulse accumulator counter can be read or written at any time.

The port A bit 7 I/O pin can be configured as a clock, in event counting mode, or as a gate signal to enable a free-running clock (E divided by 64) in gated accumulation mode.

Pulse Accumulator Timing

	Selected Crystal	Common XTAL Frequencies	
		4.0 MHz	**8.0 MHz**
CPU Clock	**(E)**	**1.0 MHz**	**2.0 MHz**
Cycle Time	**(1/E)**	**1000 ns**	**500 ns**
Pulse Accumulator (in Gated Mode)			
$(E/2^6)$ $(E/2^{14})$	1 count - overflow -	64.0 µs 16.384 ms	32.0 µs 8.192 ms



Pulse Accumulator Block Diagram

TMSK2 — Timer Interrupt Mask 2 **$1024**

	Bit 7	6	5	4	3	2	1	Bit 0
	TOI	RTII	PAOVI	PAII	0	0	PR1	PR0
RESET:	0	0	0	0	0	0	0	0

For bits 7, 6, 1, and 0, refer to **Main Timer.**

PAOVI — Pulse Accumulator Overflow Interrupt Enable
0 = PAOVF interrupts disabled
1 = Interrupt requested when PAOVF is set to one

PAII — Pulse Accumulator Input Edge Interrupt Enable
0 = PAIF interrupts disabled
1 = Interrupt requested when PAIF is set to one

Bits in TMSK2 correspond bit for bit with flag bits in TFLG2. Ones in TMSK2 enable the corresponding interrupt sources.

TFLG2 — Timer Interrupt Flag 2 **$1025**

	Bit 7	6	5	4	3	2	1	Bit 0
	TOF	RTIF	PAOVF	PAIF	0	0	0	0
RESET:	0	0	0	0	0	0	0	0

Clear flags by writing a one to the corresponding bit position(s).
For bits 7 and 6, refer to **Main Timer.**

PAOVF — Pulse Accumulator Overflow Flag
Set when PACNT changes from $FF to $00

PAIF — Pulse Accumulator Input Edge Flag
Set each time a selected active edge is detected on the PAI input line

PACTL — Pulse Accumulator Control **$1026**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDRA7	PAEN	PAMOD	PEDGE	DDRA3	I4/O5	RTR1	RTR0
RESET:	0	0	0	0	0	0	0	0

For bits 7 and 3, refer to **Parallel I/O**. For bits 2,1, and 0, refer to **Main Timer.**

PAEN — Pulse Accumulator System Enable
0 = Pulse Accumulator disabled
1 = Pulse Accumulator enabled

PAMOD — Pulse Accumulator Mode
0 = Event counter
1 = Gate time accumulation

PEDGE — Pulse Accumulator Edge Control

PAMOD	PEDGE	Action on Clock
0	0	PAI Falling Edge Increments the Counter
0	1	PAI Rising Edge Increments the Counter
1	0	A Zero on PAI Inhibits Counting
1	1	A One on PAI Inhibits Counting

PACNT — Pulse Accumulator Counter **$1027**

Bit 7	6	5	4	3	2	1	Bit 0
Bit 7	6	5	4	3	2	1	Bit 0

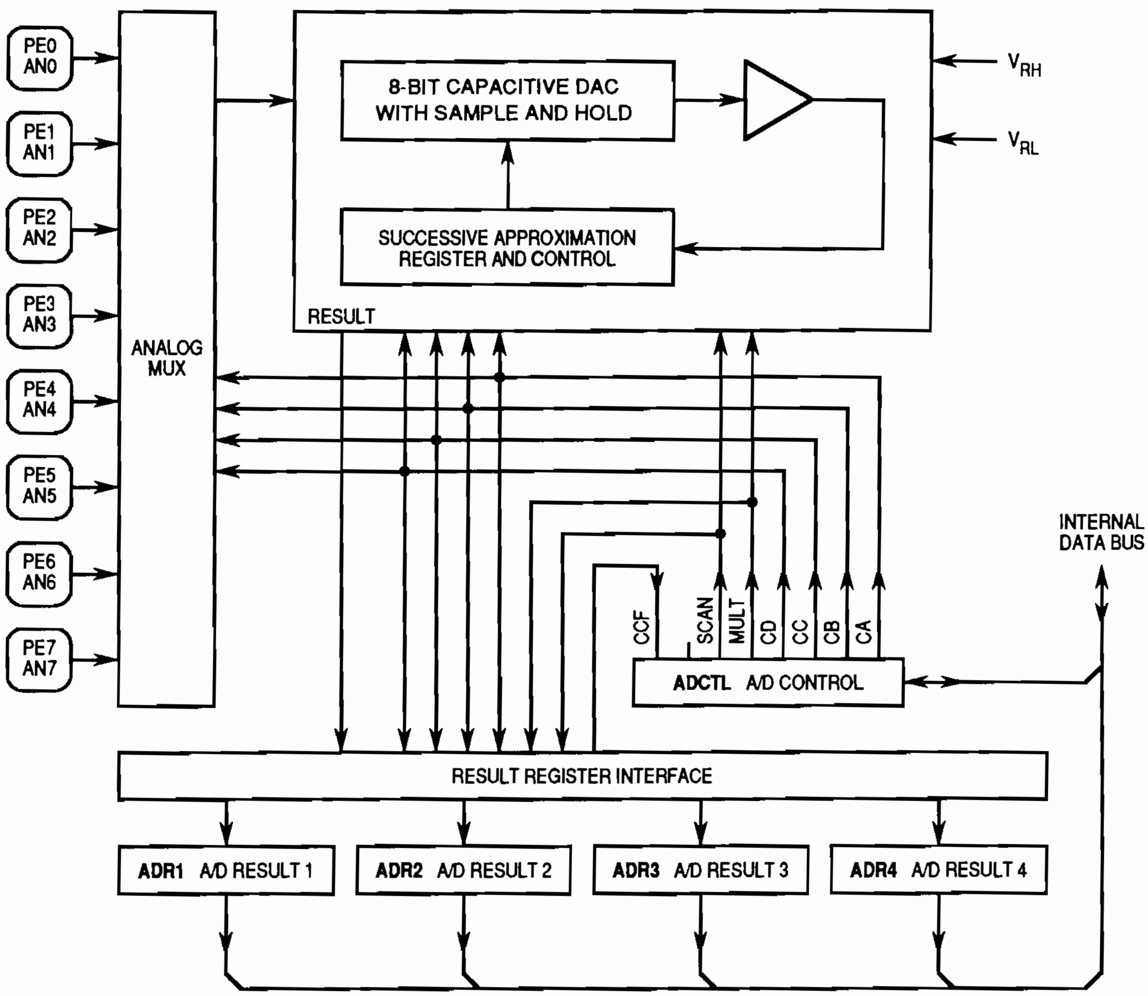
Readable and writable

A/D Converter

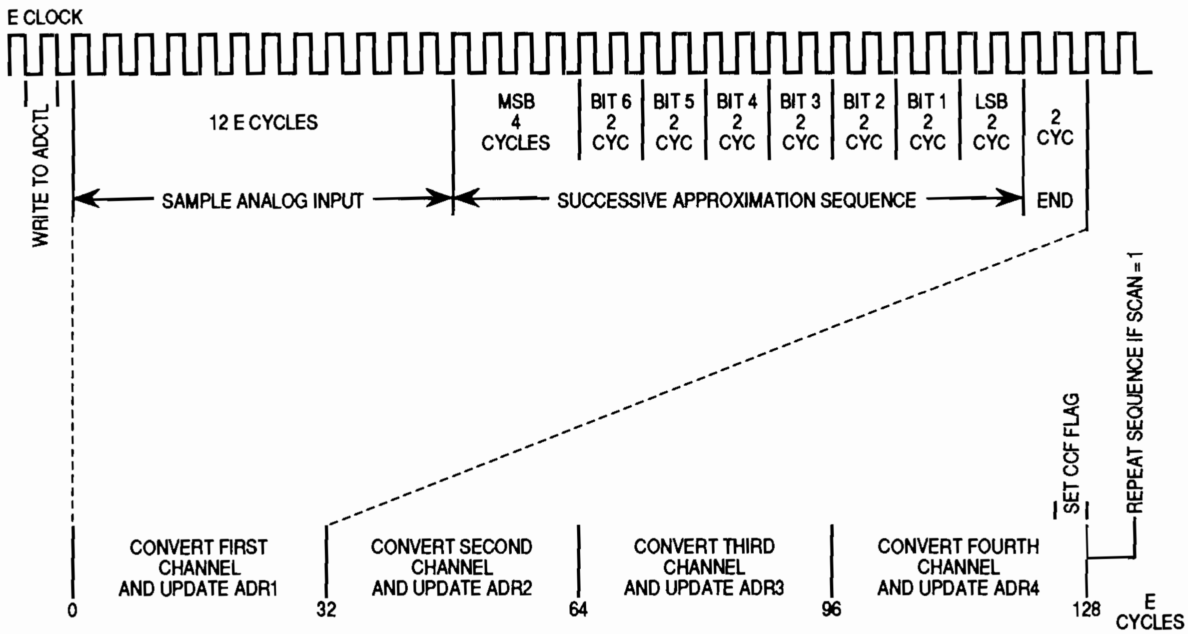
The A/D converter system uses an all-capacitive charge-redistribution technique to convert analog signals to digital values. MC68HC811E2 has an 8-channel, 8-bit, multiplexed-input, successive-approximation converter, accurate to ±1 least significant bit (LSB). It does not require external sample and hold circuits because of the type of charge-redistribution technique used.

Dedicated lines V_{RH} and V_{RL} provide the reference supply voltage inputs.

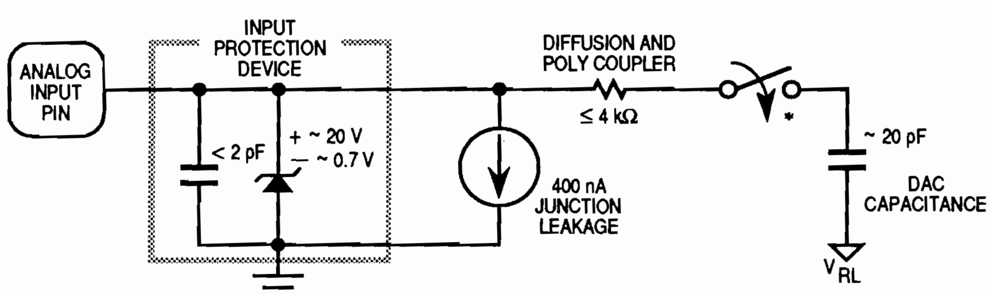
A multiplexer allows the single A/D converter to select one of 16 analog signals (eight pins plus internal signals), as shown in the table in the ADCTL register description.



A/D Converter Block Diagram



A/D Conversion Sequence



*This analog switch is closed only during the 12-cycle sample time.

Electrical Model of an Analog Input Pin (Sample Mode)

ADCTL — A/D Control/Status **$1030**

	Bit 7	6	5	4	3	2	1	Bit 0
	CCF	0	SCAN	MULT	CD	CC	CB	CA
RESET:	U	0	U	U	U	U	U	U

CCF — Conversions Complete Flag
Set after the fourth conversion in an A/D conversion cycle.
Cleared when ADCTL is written.

SCAN — Continuous Scan Control
0 = Do four conversions and stop
1 = Convert four channels in selected group continuously

MULT — Multiple Channel/Single Channel Control
0 = Convert single channel selected
1 = Convert four channels in selected group

CD–CA — Channel Select D through A

A/D Converter Channel Assignments

Channel Select Control Bits				Channel Signal	Result in ADRx if MULT = 1
CD	CC	CB	CA		
0	0	0	0	AN0	ADR1
0	0	0	1	AN1	ADR2
0	0	1	0	AN2	ADR3
0	0	1	1	AN3	ADR4
0	1	0	0	AN4*	ADR1
0	1	0	1	AN5*	ADR2
0	1	1	0	AN6*	ADR3
0	1	1	1	AN7*	ADR4
1	0	X	X	Reserved	—
1	1	0	0	V_{RH}**	ADR1
1	1	0	1	V_{RL}**	ADR2
1	1	1	0	$(V_{RH})/2$**	ADR3
1	1	1	1	Reserved**	ADR4

* Not bonded in 48-pin model
** Used for factory testing

ADR1–ADR4 — A/D Results $1031–$1034

$1031	Bit 7	6	5	4	3	2	1	Bit 0	**ADR1**
$1031	Bit 7	6	5	4	3	2	1	Bit 0	**ADR2**
$1031	Bit 7	6	5	4	3	2	1	Bit 0	**ADR3**
$1031	Bit 7	6	5	4	3	2	1	Bit 0	**ADR4**

Analog Input to 8-Bit Result Translation Table

	Bit 7	6	5	4	3	2	1	Bit 0
% (1)	50%	25%	12.5%	6.25%	3.12%	1.56%	0.78%	0.39%
Volts (2)	2.500	1.250	0.625	0.3125	0.1562	0.0781	0.0391	0.0195

(1) % of V_{RH}–V_{RL} (2) Volts for $V_{RL} = 0$; $V_{RH} = 5.0$ V

OPTION — System Configuration Options $1039

	Bit 7	6	5	4	3	2	1	Bit 0
	ADPU	CSEL	IRQE*	DLY*	CME	0	CR1*	CR0*
RESET:	0	0	0	1	0	0	0	0

*Can be written only once in first 64 cycles out of reset in normal modes,or at any time in special modes.

ADPU — A/D Power Up
- 0 = A/D powered down
- 1 = A/D powered up

CSEL — Clock Select
- 0 = A/D and EEPROM use system E clock
- 1 = A/D and EEPROM use internal RC clock

For bits 5–0, refer to **Resets and Interrupts**.

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MC68HC811E2
BR780/D

A30065 PRINTED IN USA 3/91 IMPERIAL LITHO 78170 18,000 MCU YGACAA